Claim 20 defines an electronic system, Figures 15-24. The System includes a first circuit, Figures 15A, 16A, 19D, 20A, dies 1-57; and a second circuit, Figure 16A, selectors 161, Figure 20A, selectors 201.

The first circuit has a mode input lead, Figure 16B, MODE, Figure 20B, MODE, receiving a mode signal to place the first circuit in one of a first and second mode.

The second circuit has a mode output lead, Figure 16B, MODE, Figure 20B, MODE, connected to the mode input lead of the first circuit. The second circuit has first and second clock leads, Figure 16B, S1, S2, Figure 20B, S1, S2, separate from the first circuit. At least one of the clock leads receives a clock signal that controls a mode signal formed on the mode output lead.

Claim 21 defines that the first circuit includes functional circuitry, Figure 1, the first mode is a functional mode and the second mode is a by-pass mode.

Claim 22 defines that the second circuit is a die selector circuit 161, 201 that includes D-type flip-flops, AND gates, OR gates and delay elements. See Figure 24G for the D-type flip-flops, AND gates, OR gates and delay elements.

Claim 24 defines that the second circuit includes clock input and output buffers and a state machine. See Figure 24F for the clock input and output buffers and the state machine.

Claim 25 defines that the second circuit includes third and fourth clock leads, Figure 20B, S3, S4, separate from the first

circuit and at least one of the four clock leads receives a clock signal that controls the mode signal.

Claim 26 defines that the second circuit includes third and fourth clock leads separate from the first circuit, clock input buffers, clock output buffers and a state machine. See Figures 24D and 24E.

Claim 27 defines an electronic circuit. See Figures 24D and 24F.

A first clock lead S1 connects to first input 243 and output 247 buffers.

A second clock lead S2 connects to second input 245 and output 249 buffers.

A mode lead connects to a mode output device 259.

A state machine 273 connects to the first and second input and output buffers 243-247 and connects to the mode output device 259.

Claim 28 defines a first connection from the first input buffer, Figure 24F, 243 to the second output buffer 249 and a second connection from the second input buffer 245 to the first output buffer 247.

Claim 29 defines that the state machine, Figure 24G, has inputs connected to the outputs of the first and second input

buffers 243, 245 and has outputs, S1ENA, S2ENA, connected to control the first and second output buffers 247, 249.

With this explanation, claims 20-29 were supported by the specification as originally filed. The claims were always definite under 35 USC 112, second paragraph and are described and enabled under 35 USC 112, first paragraph.

Applicant respectfully requests withdrawal of the final rejection and examination of the claims on their merits.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination.

Respectfully submitted,

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